Investigation on Molding Void Issue in System-in-Package Modules

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Abstract

Plastic encapsulation is a key feature for System-in-Package (SiP) technology as it provides robust mechanical protection and structural support for all the electronic components enclosed within the package. This allows a highly compact design with minimal component-to-component spacing without compromising long-term reliability and performance. However, as the density and complexity of SiP modules continue to escalate, the issue of molding voids and other internal defects is emerging as an increasingly significant concern. In this paper, factors stemming from the encapsulation process that could affect the formation of molding voids and related defects are discussed, and promising solutions to mitigate this issue are also proposed.

1. Introduction

Over the past decade, the enthusiasm over System-in-Package technology has been rapidly spreading from semiconductor community and Outsourced Semiconductor Assembly and Testing (OSAT) companies to a broader sector of the consumer electronics industry [1-5]. More and more consumer electronic companies and Original Equipment Manufacturer (OEM) companies regard SiP as the alternative solution to replace the traditional Printed Circuit Board Assembly (PCBA) based design, especially when it comes to hearable and wearable electronic products, Internet-of-Things (IoTs), and high-end portable devices. The advantages of SiP, such as miniaturization, better electrical and RF performance, and excellent reliability, is built based on a series features of this technology. For example, it leverages semiconductor manufacturing processes to realize a higher level of integration within a miniaturized form factor. It also uses thin layer metallic coating with thickness in micrometer range instead of the metal lid with thickness in millimeter range to achieve electromagnetic interference (EMI) shielding. Amongst these advanced features, the molding compound encapsulation is the most important one for SiP as it builds the foundation for all the others [5~7]. The encapsulation structure provides protections to all the components inside as well as their interconnections from the external forces and environmental hazards, such as moisture or chemical ingress. Therefore, the SiP technology can reduce the size of the solder joint area and the space between two components.

While plastic encapsulation has been a well-established technology in Integrated Circuit (IC) packaging for decades, SiP technology introduces new challenges regarding defect formation during the molding process [8~12]. The high complexity, dense arrangement of components and interconnections, and advanced level of integration inherent to SiP modules significantly increase the risk of molding voids

and other internal defects, such as solder extrusion. Both molding voids and solder extrusion are undesirable defects that can undermine the integrity and quality of SiP products. Addressing these issues is crucial to ensure the reliable and efficient manufacturing of these advanced packages.

In this study, a double-sided SiP module was developed and utilized as a test vehicle to evaluate the impact of different molding conditions, including transfer molding and compression molding, on the severity of molding voids and other defect modes. Various types of failure modes induced during the SiP manufacturing process and their respective failure mechanisms are discussed in detail. Additionally, the effectiveness of different detection methods in identifying these internal defects was assessed and evaluated within the scope of this study.

2. Test Vehicle and Experiment Plan

In this study, a double-sided SiP was used as a test vehicle to evaluate the impact of molding process to the voiding issue. The molding compound encapsulates both the top and bottom sides of the SiP substrate. On the bottom side, two frame boards function as interposers, enabling the connection between the SiP and the system main board. Numerous electronic components are populated on both the top and bottom surfaces of the substrate, and encapsulated within the molding compound. This SiP has a very high level of integration and a complex internal structure. It consists different types of packaging structures, including silicon die, wafer level chip scale package (WLCSP), ball grid array (BGA) package, and various passive components. Its general manufacturing process is demonstrated in Figure 1. All the samples are prepared by two different molding processes, transfer molding and compression molding, while all the other processes, such as surface mount, EMI shielding sputtering, singulation, remain the same. After assembly, all the samples are examined by a series of tests, including Scanning Acoustic Microscope (SAM) inspection, X-ray inspection, and functional test. All the failed units will be collected and further failure analysis will be carried out on those units.

3. Results and Discussions

3.1. Defect in Transfer Molding

In the transfer molding process, the molten molding compound flows over the entire SiP panel inside the mold cavity. To reach the component area, it has to navigate through long and narrow channels, which increases the likelihood of air entrapment and void formation. After SiP assembly, a 2D X-ray inspection was conducted to examine the entire SiP area, revealing a hairline solder extrusion under a particular IC component, as shown in Figure 2. The overall failure rate was 15%. The defective units were subjected to parallel lapping (p-lapping) and cross-sectional analysis to expose the defects, with the results shown in Figures 3 and 4. Both figures clearly demonstrate the presence of molding voids surrounding the defective solder joints. This evidence suggests that these voids originated during the transfer molding process, providing a pathway for the molten solder to bridge with adjacent solder balls during the subsequent reflow process, ultimately causing functional failure.

Figure 2. X-ray Image of Failed SiP Unit

Figure 3. The P-lapping Result at the Solder Extrusion Location

Figure 4. The Cross-Section Result at the Solder Extrusion Location

Computational mold flow analysis was conducted through commercial software tool to evaluate the molding void risk in transfer molding process based on current SiP layout design. The advancement of the liquid molding compound inside the mold chase was simulated and the result is schematically demonstrated in Figure 5. As seen in the picture, there are two major components on SiP bottom side, "Chip A" and "Chip B". Chip A, where the solder extrusion was found, is a waferlevel chip-scale package (WLCSP), while Chip B is a quad flat package (QFP). Chip A has both larger size (4.24x4.24 mm²) and higher pin count (114 pin count), and it is surrounded by numerous passive components. When the liquid molding compound flows across the panel, it can be observed

that the flow is impeded by Chip A. This is because the molten mold compound has to overcome the resistance posed by the relatively larger number of package solder balls on Chip A. As a result, the area underneath Chip A carries the highest risk for molding void defects. In other words, Chip A has the largest chip size and the highest number of solder bumps, which attributes provide greater resistance to the mold flow, slowing down the flow speed at this area compared to other locations on the substrate, such as the area near Chip B. Moreover, Chip A is surrounded by numerous passive components, further hindering the molding flow and making it more difficult for air to escape. Therefore, it is reasonable to conclude that the simulation results align with the observations from actual production runs.

(a) Liquid molding compound starts to flow onto the SiP panel

(b) Liquid molding compound overcomes Chip A

(c) Reversed flow is created

(d) Void appears underneath Chip A component Figure 5. Illustration of Mold Flow Behavior

3.2. Defect in Compression Molding

The compression molding uses a different approach to encapsulate the SiP test vehicle, as schematically

demonstrated in Figure 6. The upper mold holds the SiP panel after all the electronic component being populated, while the lower mold contains the powder of molding compound inside the cavity. When temperature increase, the resin power melted into liquid format, then the SiP panel gets immersed into the cavity with a controlled speed. After the two molds gets clamped, the temperature will gradually decrease and the molding compound will solidify. In compression molding, there is no molding flow inside the mold cavity. It allows the SiP module to incorporate sophisticated structures, such as wire bonding, and it also reduces the risk of generating molding voids. However, there are still 0.5% failure caught in functional test. Failure analysis was conducted to understand the failure symptom as well as the root cause.

Figure 6. Illustration of Compression Molding

A 3D Computed Tomography (CT) scan was employed to investigate the internal condition of the failed System-in-Package (SiP) module, as no anomalies were detected during SAM and 2D X-ray inspection. As shown in Figure 7, indications of defects were observed beneath several Wafer-Level Chip Scale Package (WLCSP) and Ball Grid Array (BGA) components Further cross-sectional analysis confirms that these defects are instances of solder extrusion, as shown in Figure 8. It can be seen that, in contrast to the defects encountered in the transfer molding process, no molding voids were presented underneath these components. Also, the solder extrusion manifests itself as a thin layer between the molding compound and the substrate layer. This observation implies that the underlying root cause contributing to the formation of solder extrusion in the compression molding process is distinct from the mechanisms discussed in the preceding sections. Based on this phenomenon, it is suspected that the flux residual remains on the substrate surface after SMT and flux cleaning process. In the subsequent reflow process (such as reballing), the solder penetrates into the flux residuals, leading to the formation of bridging with the adjacent balls. The validity of this hypothesis was verified through an experimental investigation. Samples were prepared following the same manufacturing process, except that the flux cleaning step after SMT was intentionally skipped to allow flux residues to remain on the substrate surface. Subsequently, these samples underwent X-ray inspection and cross-sectional analysis. The results revealed the presence of the same type of thin-layer solder extrusion between the molding compound and the substrate, therefore supporting the proposed hypothesis.

Figure 7. CT-Scan on Defective SiP

Figure 8. Cross-section of Solder Extrusion

3. Post-Molding Reflow

Figure 9. Failure Mechanism of Thin Layer Solder Extrusion in Compression Mold

4. Conclusions

In this paper, the issue of molding voids and other internal defects in System-in-Package (SiP) technology are investigated, focusing on the impact of different molding technology. A double-sided SiP module with a high level of integration and complex internal structure are used as test vehicle.

- In transfer molding, the molding flow simulation and failure analysis showed that the molding voids tend to form under components with larger size and higher pin count, like the WLCSP chip. This is due to the higher resistance posed by these components to the molding flow.
- In compression molding, no molding voids were found, but a different type of defect - thin-layer

solder extrusion - was observed. This was attributed to the presence of flux residues on the substrate surface after the SMT and flux cleaning process.

- The paper discussed various failure mechanisms associated with these defects and evaluated the effectiveness of different inspection techniques, like X-ray, SAM, and cross-sectioning, in identifying them.
- The study suggests that addressing these manufacturing challenges, through optimized molding process parameters and design, is crucial to ensuring the reliable and efficient production of advanced SiP modules.

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